WHAT IS CLAIMED IS:

1. A semiconductor device in which a switching element for allowing a current to flow to a load and a circuit for driving the switching element are formed on a common substrate,

wherein said switching element is a first insulated gate transistor which comprises:

a first semiconductor region of a second conductive type disposed at one main surface of a semiconductor substrate of a first conductive type;

a second semiconductor region of the first conductive type disposed within the first semiconductor region;

a first gate electrode disposed on a surface in which a pn junction between the second semiconductor region and the first semiconductor region terminates, through an insulating film;

a first source region of the second conductive type which is disposed on one end portion side of said first gate electrode within said second semiconductor region; and

a first drain region of the second conductive type which is disposed within said first semiconductor region; and

wherein said circuit for driving said switching element comprises a second insulated gate transistor having a characteristic different from that of said

first insulated gate transistor.

2. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor constitutes a level shift circuit that generates a drive voltage applied to said first gate electrode.

3. The semiconductor device as claimed in claim 1, wherein a drain region of said second insulated gate transistor includes a low impurity concentration region.

4. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor constitutes a level shift circuit that generates a drive voltage applied to said first gate, and a low impurity concentration region is disposed within a drain region of said second insulated gate transistor.

5. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor is a source follower transistor that constitutes a level shift circuit that generates a drive voltage applied to said first gate through a CMOS circuit.

6. The semiconductor device as claimed in claim 1, wherein a well potential of said second insulated gate transistor is different from both a source potential and a drain potential.

7. The semiconductor device as claimed in claim 1, wherein a drain region of said second insulated gate transistor has a low impurity concentration region that is formed to be shallower than said first semiconductor region.

8. The semiconductor device as claimed in claim 1, wherein a drain region of said second insulated gate transistor has a low impurity concentration region having the same depth as that of said first semiconductor region.

9. The semiconductor device as claimed in claim 1, wherein said second semiconductor region is formed deeper than said first semiconductor region.

10. The semiconductor device as claimed in claim 9, wherein a plurality of first insulated gate transistors are arranged in an array without dedicated element isolation regions being interposed therebetween.

11. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor is an MOS transistor of the first conductive type which constitutes a low-voltage CMOS circuit.

12. The semiconductor device as claimed in claim 1, wherein said circuit for driving said switching element comprises a low-voltage CMOS circuit having said second insulated gate transistor, and a high-voltage CMOS circuit that is controlled by said low-voltage CMOS circuit; and

wherein an MOS transistor of the first conductive type which constitutes said high-voltage CMOS circuit is a DMOS transistor produced in the same process as that for forming said first insulated gate transistor.

13. The semiconductor device as claimed in claim 12, further comprising a level shift circuit that generates a drive voltage applied to said first gate electrode through said high-voltage CMOS circuit.

14. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor includes source and drain regions of the first conductive type which are formed within said

well of the second conductive type.

15. The semiconductor device as claimed in claim 1, wherein an electro-thermal converter that functions as said load is connected to a drain of said switching element and is integrated.

16. The semiconductor device as claimed in claim 1, wherein said characteristic is at least one selected from a threshold value, a breakdown voltage and a substrate current.

17. A semiconductor device in which a switching element for allowing a current to flow to a load and a circuit for driving the switching element are formed on a common substrate, wherein:

said switching element is formed of a DMOS transistor; and

said circuit for driving the switching element includes an MOS transistor having a characteristic different from that of said DMOS transistor.

18. The semiconductor device as claimed in claim 17, wherein said MOS transistor is of the same conductive type as that of said DMOS transistor.

19. The semiconductor device as claimed in

claim 17, wherein a drain region of said MOS transistor includes a low impurity concentration region.

20. The semiconductor device as claimed in claim 17, wherein said MOS transistor constitutes a level shift circuit that generates a drive voltage applied to a gate electrode of said DMOS transistor, and a low impurity concentration region is disposed within the drain region.

21. The semiconductor device as claimed in claim 17, wherein said MOS transistor is a source follower transistor that constitutes a level shift circuit that generates a drive voltage applied to the gate electrode of said DMOS transistor through a CMOS circuit.

22. The semiconductor device as claimed in claim 17, wherein a well potential of said MOS transistor is different from both a source potential and a drain potential.

23. The semiconductor device as claimed in claim 17, wherein a drain region of said MOS transistor has a low impurity concentration region formed to be shallower than a base region that

becomes a channel of said DMOS transistor.

24. The semiconductor device as claimed in claim 17, wherein a drain region of said MOS transistor has a low impurity concentration region having the same depth as that of a base region that becomes a channel of said DMOS transistor.

25. The semiconductor device as claimed in claim 17, wherein a base region that becomes a channel of said DMOS transistor is formed to be deeper than a lightly doped drain region.

26. The semiconductor device as claimed in claim 17, wherein a plurality of said DMOS transistors are arranged in an array without dedicated element isolation regions being interposed therebetween.

27. The semiconductor device as claimed in claim 17, wherein said MOS transistor is an MOS transistor of the first conductive type which constitutes a low-voltage CMOS circuit.

28. The semiconductor device as claimed in claim 17, wherein said circuit for driving said switching element comprises a low-voltage CMOS

circuit having said MOS transistor, and a high-voltage CMOS circuit that is controlled by said low-voltage CMOS circuit; and

wherein an MOS transistor of the first conductive type which constitutes said high-voltage CMOS circuit is a DMOS transistor produced in the same process as that for producing said DMOS transistor.

29. The semiconductor device as claimed in claim 28, further comprising a level shift circuit that generates a drive voltage that is applied to the gate electrode of said DMOS transistor that functions as said switching element, through said high-voltage CMOS circuit.

30. The semiconductor device as claimed in claim 17, wherein said DMOS transistor includes source and drain regions of the first conductive type which are formed within said well of the second conductive type.

31. The semiconductor device as claimed in claim 17, wherein an electro-thermal converter that functions as said load is connected to a drain of said DMOS transistor into integration.

32. The semiconductor device as claimed in claim 17, wherein said DMOS transistor comprises:

a first semiconductor region of a second conductive type disposed at one main surface of a semiconductor substrate of a first conductive type;

a second semiconductor region of the first conductive type disposed within the first semiconductor region;

a first gate electrode disposed on a surface in which a pn junction between the second semiconductor region and the second semiconductor region terminates, through an insulating film;

a first source region of the second conductive type which is disposed on one end portion side of said first gate electrode within said second semiconductor region; and

a first drain region of the second conductive type disposed within said first semiconductor region.

33. The semiconductor device as claimed in claim 1, wherein said second insulated gate transistor has an on resistance that is equal or greater, and an operation breakdown voltage that is 2/3 or lower, as compared with those of said first insulated gate transistor.

34. The semiconductor device as claimed in

claim 1, wherein said second insulated gate transistor has an on resistance that is equal or grater, and the maximum substrate current in an operation range which is 10 times or higher, as compared with those of said first insulated gate transistor.

35. The semiconductor device as claimed in claim 17, wherein said MOS transistor has an on resistance that is equal or greater, and an operation breakdown voltage that is 2/3 or lower, as compared with those of said DMOS transistor.

36. The semiconductor device as claimed in claim 17, wherein said MOS transistor has an on resistance that is equal or grater, and the maximum substrate current in an operation range which is 10 times or higher, as compared with those of said DMOS transistor.

37. A liquid jet apparatus that jets a liquid by using a heat generated from an electro-thermal converter, said apparatus comprising:

a semiconductor device as claimed in claim 1;

a discharge opening disposed in correspondence with the electro-thermal converter that becomes the load;

a container that contains the liquid that is supplied onto the electro-thermal converter; and

a power circuit for supplying a power voltage to said semiconductor device.

38. A liquid jet apparatus that jets a liquid by using a heat generated from an electro-thermal converter, said apparatus comprising:

a semiconductor device as claimed in claim 17;

a discharge opening disposed in correspondence with the electro-thermal converter that becomes the load;

a container that contains the liquid that is supplied onto the electro-thermal converter; and

a power circuit for supplying a power voltage to said semiconductor device.

39. A method of manufacturing a semiconductor device in which a switching element and a circuit for driving the switching element are formed on a common substrate, said method comprising the steps of:

forming a first semiconductor region of a second conductive type on a surface of a first conductive type semiconductor substrate;

forming a gate insulating film on the first semiconductor region;

forming a first gate electrode on the surface

of said first semiconductor region through said gate insulating film, and a second gate electrode on the surface of said semiconductor substrate through said gate insulating film;

forming a second semiconductor region of a first conductive type which have a higher concentration than that of the first semiconductor region, within said first semiconductor region by ion implantation of first conductive type impurities with said first gate electrode as a mask;

forming a lightly doped drain region of the second conductive type in said semiconductor substrate by ion implantation of impurities of the second conductive type, with said second gate electrode as a mask; and

forming a first source region of the second conductive type on a surface side of said second semiconductor region by ion implantation with said first gate electrode as a mask, forming a first drain region of the second conductive type on a surface side of said first semiconductor region, forming a second source region of the second conductive type on a surface side of said semiconductor substrate by ion implantation, and forming a second drain region of the second conductive type so as to be apart from an end portion of said lightly doped drain region on the second gate electrode side.

40. The method of manufacturing a semiconductor device as claimed in claim 39, wherein said second semiconductor region is formed so as to be higher in concentration than said first semiconductor region and deeper than said first semiconductor region, in order to electrically insulate said first semiconductor region by ion implantation of the first conductive impurities with said first gate electrode as a mask and a heat treatment.

41. A method of manufacturing a semiconductor device in which a switching element and a circuit for driving the switching element are formed on a common substrate, said method comprising the steps of:

forming a plurality of first semiconductor regions of a second conductive type on a surface of a semiconductor substrate of a first conductive type;

forming a gate insulating film on the plurality of first semiconductor regions;

forming a first gate electrode on a surface of one of said plurality of first semiconductor regions through said gate insulating film, and a second gate electrode on a surface in which a pn junction between said semiconductor substrate and another one of said plurality of first semiconductor regions terminates, through said gate insulating film;

forming a second semiconductor region of the first conductive type within one of said plurality of first semiconductor regions by ion implanting impurities of the first conductive type, with said first gate electrode as a mask;

forming a first source region of the second conductive type by ion implanting impurities of the second conductive type with said first gate electrode on the surface side of said second semiconductor region as a mask, forming a first drain region of the second conductive type on a surface side of said first semiconductor region, forming a second source region of the second conductive type on a surface side of said semiconductor substrate, and forming a second drain region of the second conductive type on the surface side of said first semiconductor region so as to be apart from a pn junction between said semiconductor substrate and said first semiconductor region.

42. The method of manufacturing a semiconductor device as claimed in claim 41, wherein said second semiconductor region is formed so as to be higher in concentration than said first semiconductor region and deeper than said first semiconductor region, in order to isolate one of said plurality of first semiconductor regions.

43. A liquid jet apparatus that jets a liquid by using a heat generated from an electro-thermal converter, said apparatus comprising:

a semiconductor device as claimed in claim 1; and

a discharge opening disposed in correspondence with the electro-thermal converter that becomes the load.

44. A liquid jet apparatus that jets a liquid by using a heat generated from an electro-thermal converter, said apparatus comprising:

a semiconductor device as claimed in claim 17; and

a discharge opening disposed in correspondence with the electro-thermal converter that becomes the load.